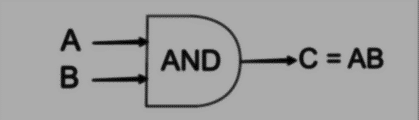
**LAB # 01**

**Objective:**

To design AND, OR, NAND, NOR, NOT gate in Verilog by using gate level modelling.

**For AND Gate**

**Circuit diagram:**

**Coding:**

//Design Module

module gate(c,a,b);

input a,b;

output c;

and a1(c,a,b);

endmodule

//Stimulax Module

module aazib;

reg a,b;

wire c;

gate h1(c,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

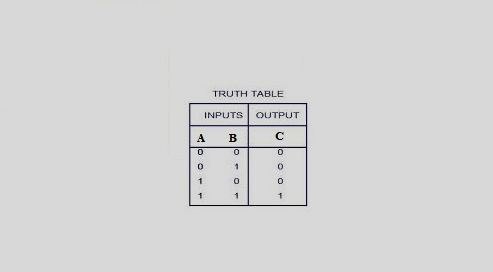
a=1'b1; b=1'b1;

#20

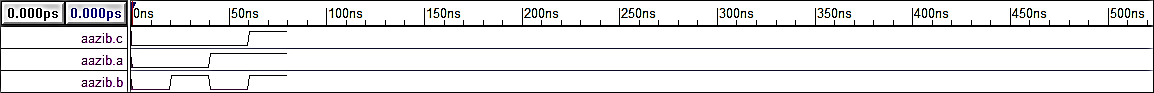
$finish;

end

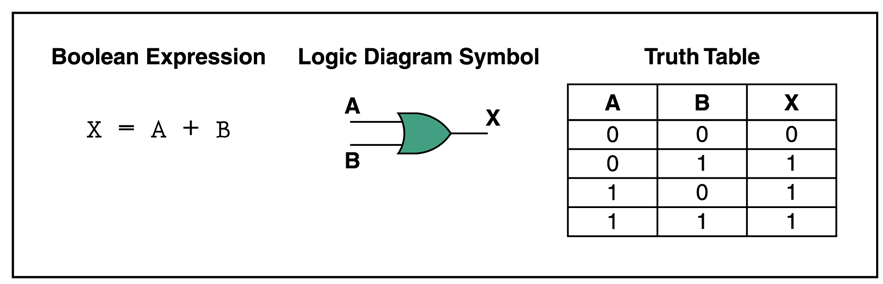
endmodule

** Truth Table:**

**Results (Timing diagram) :**



**For OR Gate**

**Circuit diagram:**

**Coding:**

//Design Module

module gate(x,a,b);

input a,b;

output c;

or a1(x,a,b);

endmodule

//Stimulax Module

module aazib;

reg a,b;

wire x;

gate h1(x,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

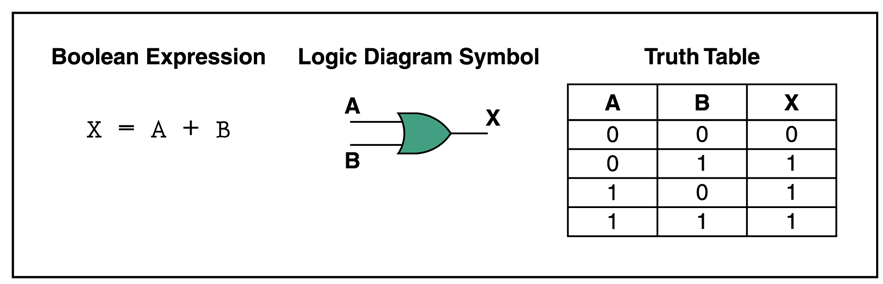
a=1'b1; b=1'b1;

#20

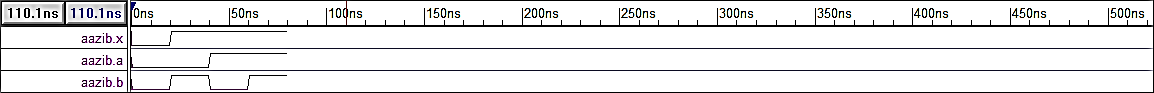
$finish;

end

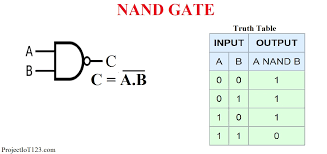
endmodule

**Truth Table:**

**Results (Timing diagram) :**



**For NAND Gate**

**Circuit diagram:**

**Coding:**

//Design Module

module gate(c,a,b);

input a,b;

output c;

nand a1(c,a,b);

endmodule

//Stimulax Module

module aazib;

reg a,b;

wire c;

gate h1(c,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

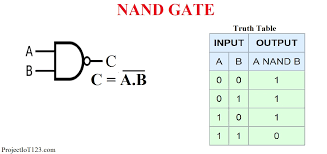
a=1'b1; b=1'b1;

#20

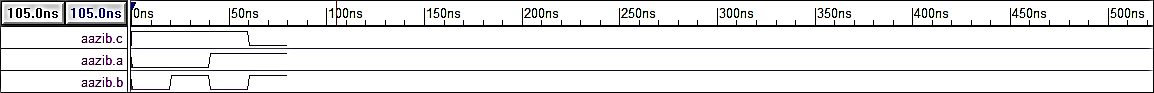
$finish;

end

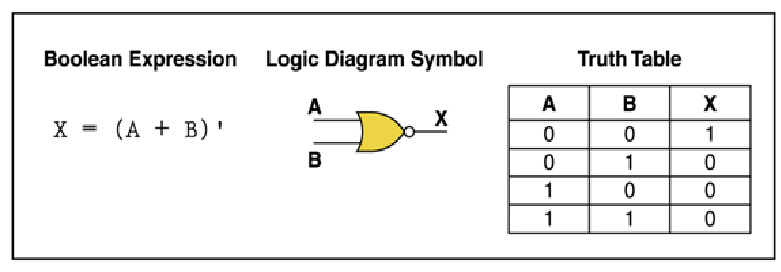
endmodule

**Truth Table:**

**Results (Timing diagram) :**



**For NOR Gate**

**Circuit diagram:**

**Coding:**

//Design Module

module gate(x,a,b);

input a,b;

output x;

nor a1(x,a,b);

endmodule

//Stimulax Module

module aazib;

reg a,b;

wire c;

gate h1(x,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

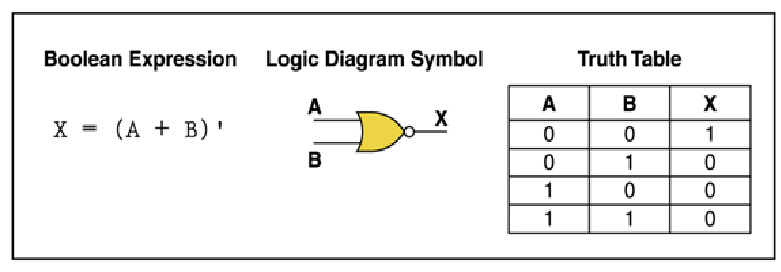
a=1'b1; b=1'b1;

#20

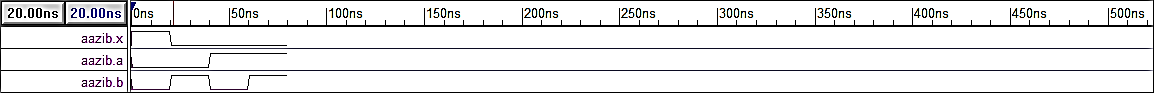
$finish;

end

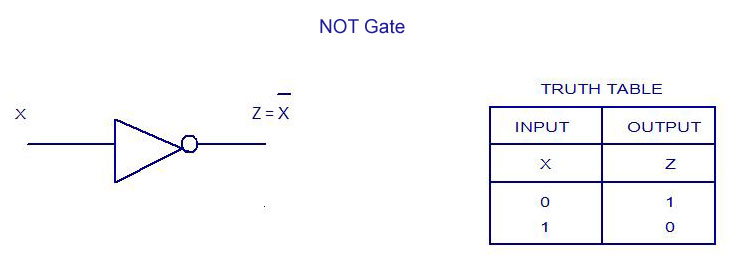
endmodule

**Truth Table:**

**Results (Timing diagram) :**



**For NOT Gate**

**Circuit diagram:**

**Coding:**

//Design Module

module gate(z,x);

input x;

output z;

not a1(z,x);

endmodule

//Stimulax Module

module aazib;

reg x;

wire z;

gate h1(z,x);

initial

begin

a=1'b0;

#20

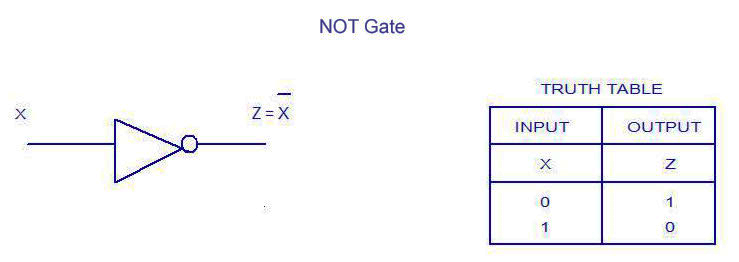
a=1'b1;

#20

$finish;

end

endmodule

**Truth Table:**

**Results (Timing diagram) :**

